JOB DESCRIPTION – Sr. Staff FPGA Engineer

Location: Rolling Meadows, IL

Date: July 14th, 2021

Scope of Responsibilities & Position Expectations

The Rolling Meadows PMP FPGA team is looking for a lead FPGA developer who will be responsible for the following items:

- Contributions in all phases of product development lifecycle from conception through implementation of features, integration, and test.
- Document designs and interfaces.
- Design and Implement RF control algorithms.
- Develop and Optimize RF PHY implementation.
- Refactor existing code to improve efficiencies with respect to Timing closure and Device Fit.
- Interact and coordinate with members of other engineering and production teams.
- Assist with the diagnosis and resolution of customer problems.

Specific Knowledge/Skills

Required (Technical):

- Experience with design and analysis of static microwave wireless systems including:
 - RF MIMO and MU-MIMO OFDM Systems
 - MAC Familiarity with MAC layer design concepts
 - PHY FFT, Coding, Interleaving
- Experience with FPGA development and debug tools
 - RTL design and simulation using Verilog and VHDL
 - SDC timing constraints
 - Design methods to obtain timing closure and fit
 - FPGA design tools such as Altera Quartus, TimeQuest, SignalTap, Xilinx Vivado
 - Simulator tools such as Aldec Riviera
- Experience with SoC architectures such as Altera Cyclone V SoC and Xilinx Zynq
- Strong analytical, problem solving and creative abilities.
- Good verbal and written communication skills.
- Interface with other Engineering teams (Hardware, System Test, Marketing, Documentation).





Desirable:

- Knowledge of networking protocols such as TCP/IP stack.
- Knowledge of RF principles.
- Experience with C programming.
- Experience using Oscilloscope and Spectrum Analyzer.
- Experience of working under distributed version control (e.g. GIT or Mercurial).
- Experience of working in cross site, multinational teams.
- Experience with scripting languages like TCL, Python, Linux Shells.